Allegro Sigrity PI Solution

Streamlining the creation of power delivery networks on high-speed and high-current PCBs and IC packages

The Cadence® Allegro® Sigrity™ PI integrated design and analysis environment streamlines the creation of power delivery networks (PDNs) on high-speed and high-current PCB systems and IC packages. A range of capabilities—from basic to advanced—enable designers and electrical engineers to explore, optimize, and resolve issues related to electrical performance at all stages of the design cycle. By enabling an electrical constraint-driven design flow, this unique environment accelerates the time-to-design success while reducing the overall cost of end products.

Allegro Sigrity PI Solution

The Allegro Sigrity PI solution provides a scalable, cost-effective pre- and post-layout system PDN design and analysis environment, including both first-order and advanced analysis for the board, package, and system levels. The Allegro Sigrity PI Base integrates tightly with Cadence PCB and IC package layout editors and with Cadence Allegro Design Authoring, enabling front-to-back, constraint-driven PDN design for PCB and IC package design.

Allegro Sigrity PI solution addresses the design challenges presented by increasing design density, faster data throughput, and shrinking product design schedules by enabling designers to address power delivery network issues throughout the design process. This approach allows design teams to eliminate time-consuming iterations at the back end of a design process.

Power and ground networks in a PDN can be modeled with a hybrid solver or a 3D full-wave solver, depending on the detail available and the expertise of the user.

Decoupling capacitor placement is guided through power integrity constraint sets (PI Csets) that associate capacitors with components and define capacitor placement within a constrained distance and on the same or opposite side of the design as the component.

Key Capabilities

- Highly integrated design and analysis environment removes the need for error-prone and time-consuming manual design translation
- Intuitive in-design analysis tools enable a design methodology that streamlines post-route signoff verification through a consistent front-to-back electrical constraint management environment
- DC IR drop analysis is performed in a dual window view of the design so that edits can be made in the Allegro editor while viewing the IR drop analysis
- Design-rule checking (DRC) markers are placed on the Allegro editor at the precise locations that cause DC IR drop beyond constrained limits
- IC package designs are easily assessed for design quality and characterized for use in die-to-die transient power analysis

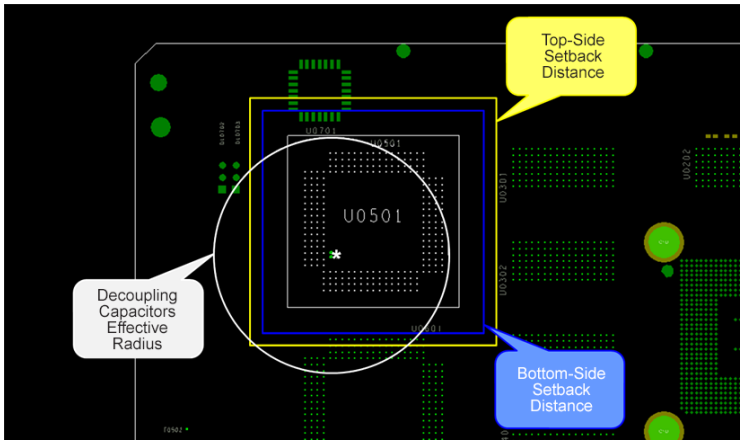

Figure 1: Power integrity constraint sets guide the placement of decoupling capacitors

Features

The Allegro design canvas features included with the Allegro Sigrity PI solution can be used to view and modify a design while analyzing an Allegro PCB or IC package design.

Integrated PDN design and analysis

To eliminate the risk of design translation issues, the Allegro Sigrity PI solution seamlessly integrates with the Allegro PCB and IC package layout editors and allows constraints and models to be tightly integrated with the design file. The power feasibility editor, which helps to select proper decoupling capacitor values, can be used at any point in the design process. The ideal methodology will use the power feasibility editor while capturing design intent, and apply PI constraint sets (PI Csets) to the decoupling capacitors chosen.

Once design intent is complete and place-and-route begins, the layout engineer follows the PI Csets captured earlier. When designing power and ground planes, DC IR drop analysis can be performed to ensure voltage levels will be maintained and current density is within guidelines.

Decoupling capacitor optimization

With all PI Csets met and DC IR drop problems resolved, the layout engineer can then turn the design over to the PI expert to run advanced power integrity analysis with the optimization and signoff option. Decoupling capacitor values and functionality are evaluated against cost and performance requirements, and recommendations for the ideal cost vs. performance scheme can then be fed back to the layout engineer.

Thermal-aware analysis

The PI expert may also choose to run advanced IR drop analysis that considers both component and joule heating of the design. Because voltage drops differently at different temperatures, signoff level accuracy needs to consider the temperature changes across the design. The PI expert can perform this signoff level IR drop analysis with the optimization and signoff option, then test recommended changes to the power and ground planes and feed them back to the layout engineer.

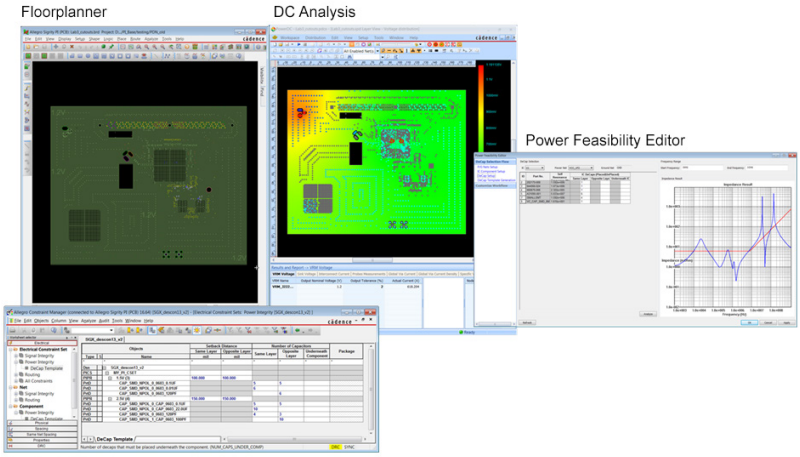

Figure 2: Allegro Sigrity PI Base creates a workflow for design teams to streamline resolution of first-order power integrity problems

AC analysis

PI experts can perform AC analysis simulations to assess voltage distribution across ground planes. Observation locations can be chosen to focus on areas of interest such as voltage levels between plane pairs and performance for specific frequency ranges. A variety of 2D and 3D visualization options enables rapid results assessment. A task-focused workflow can be customized to provide step-by-step guidance tuned for frequent analysis tasks and to establish defaults to guide new users.

The AC analysis tool also supports S-parameter model extraction of coupled signal, power, and ground and design stage EMI analysis using the hybrid solver extraction engine. The tool offers a spatial mode in which impedance can be seen spatially at specific frequencies, which is particularly useful in identifying hotspots on the board or IC package.

IC packaging assessment and model extraction methodology

The Allegro Sigrity PI solution provides an environment for the assessment, characterization, and simulations of IC package (.mcm or .sip) interconnect. Engineers can make tradeoffs to minimize cost while maximizing performance of the package module interconnect.

The electrical-assessment features are most commonly used by the package designer to gain a quick first-order evaluation of the electrical quality of the package design. Signal analysis (trace impedance and coupling checks), power/ground analysis (net-pair and per-pin properties), and DC current analysis (DC current and IR drop analysis) are available as part of the assessment capability. Assessments are accomplished with minimal electromagnetic expertise. HTML-based reports can be created showing the level of analysis that has been performed along with the results.

The IC package assessment and model extraction methodology is tightly integrated with the package design environment, and can prove particularly valuable when package design is outsourced. The electrical performance assessment features provide a quick and thorough means to assess the package design, which reduces the time before providing feedback to the package designers. When the assessment provides good results, the extraction technology is an efficient way to develop full-package models or highly accurate package-section models for use in high-frequency system-level time-domain simulation.

For more advanced analysis, package characterization engineers have access to integrated hybrid (2D/3D) and full-wave 3D field solver engines. These solvers can be used to create full-package models, or a smaller section of the package can be extracted to create high-fidelity S-parameter models. These models can be analyzed independently or passed off to system signal-integrity (SI) analysts to include the package model in their system topologies.

In addition, thermal and thermally aware IR drop analysis is available as part of the solution.

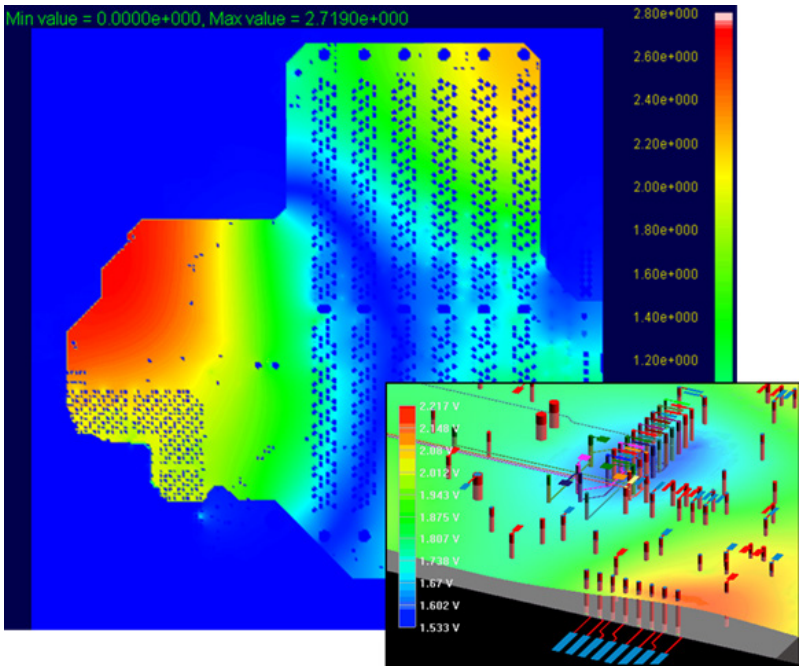

Figure 3: AC analysis offers a spatial mode that helps identify hotspots

Constraint-driven design methodology

Allegro Sigrity PI technology works seamlessly with the constraint management system of the Allegro PCB and IC packaging design tools. Design intent regarding decoupling capacitors can be captured during schematic capture in the form of a PI Cset, which can then be reused whenever a component with same decoupling scheme is used, in the same or different designs.

Benefits

- In-design and post-route PI signoff analysis integrated with the physical design flow provides optimum methodology
- Power integrity constraints capture design intent constraint-driven physical design methodology
- Scalable crosstalk analysis, from segment-based crosstalk DRCs to detailed time-domain simulation
- Hybrid (2D/3D) and full-wave 3D solvers provide extraction scalability, and enable power and ground modeling by extracting accurate models
- Electrical assessment of IC packages quickly identifies electrical faults and baselines performance metrics
- Decoupling capacitor optimization of cost vs. performance
- Both AC and thermally-aware DC analysis for signoff-accurate power integrity analysis
- Reads/writes Cadence Allegro Package Designer (.mcm) and SiP Digital Layout (.sip) files

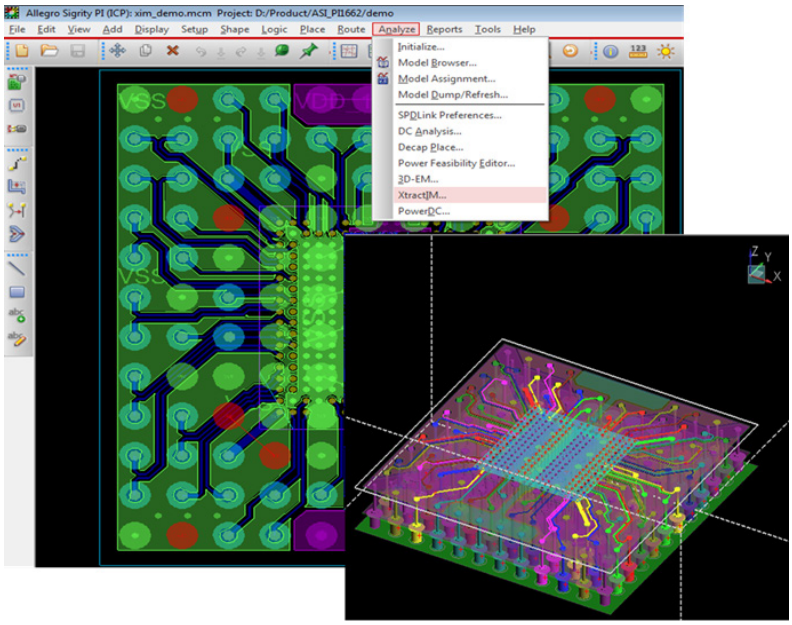

Figure 4: Package assessment and extraction is tightly integrated with the package design environment, and includes quick assessments, detailed full-package models or 3D package sections, and IR drop and thermal analysis

Operating System Support

Allegro platform technology:

- Linux
- Windows

Cadence Services and Support

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
- Cadence certified instructors teach more than 70 courses and bring their real-world experience into the classroom
- More than 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
- Cadence Online Support gives you 24x7 online access to a knowledgebase of the latest solutions, technical documentation, software downloads, and more

Allegro Sigrity PI Product Summary

Sigrity Products	Allegro Sigrity PI Base	Signoff and Optimization Option	Package Assessment/ Extraction Option
Note: An option license provides access to one product at a time			
CAD design/data translators		•	•
PowerDC™ technology		•	•
PowerSI™ technology		•	
PowerSI 3D EM Full-Wave Extraction		•	•
OptimizePI™ technology		•	
XtractIM™ technology			•

Allegro Sigrity PI Feature Summary

Features	Allegro Sigrity PI Base	Signoff and Optimization Option	Package Assessment/ Extraction Option
Static DC IR drop analysis with DRC marker back-annotation	•	•	•
IBIS 5.1 support			•
Graphical topology editor			•
Bus-level topology editor			•
Detailed HTML simulation reports	•	•	•
Post-layout selection from Allegro PCB Editor	•		
HSPICE interface			•
Constraint-driven floorplanning and placement	•		
Allegro Constraint Manager	•		
Real-time feedback on decoupling capacitor placement violations	•		
Constraint-driven routing	•		
Allegro route by pick	•		
Thermally aware static IR drop analysis		•	•
AC analysis of PCB and IC package PDNs		•	
Decoupling capacitor optimization of cost vs. performance		•	
Hybrid-solver (2D/3D) extraction		•	•
3D full-wave extraction		•	•
Signal-quality screening of routed nets		•	
Frequency domain analysis		•	•

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